

Serial No. 09/879,724
Amendment Dated May 19, 2003

Attorney Docket No. F0522
Response To Office Action Dated April 4, 2003

AMENDMENTS IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- C'
1. (Currently Amended) A semiconductor-on-insulator (SOI) structure comprising;
a semiconductor substrate;
a leaky, thermally conductive insulator material (LTCIM) layer disposed directly on the semiconductor substrate;
a semiconductor layer disposed directly on the LTCIM layer; and
active regions defined in the semiconductor layer by isolation trenches and the LTCIM layer,
wherein the LTCIM layer comprises at least one of doped amorphous silicon, undoped amorphous silicon and undoped porous silicon,
wherein when the LTCIM layer is doped amorphous silicon a dopant species is selected from one of boron, phosphorous and fluorine, and
wherein the LTCIM layer extends over an entire lateral dimension of the semiconductor substrate.
 2. (Original) The SOI structure according to claim 1, wherein the semiconductor substrate material is silicon (Si), silicon carbide (SiC), silicon germanium (SiGe) or any other semiconductive material.
 3. (Original) The SOI structure according to claim 1, wherein the LTCIM layer has a thermally conductivity value between about 30 W/mK to about 170 W/mK.
 4. (Canceled)

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5. (Currently Amended) The SOI structure according to claim 4 1, wherein the LTCIM layer preferably has a resistivity value 10 Ohms-cm or greater.

6.-16. (Canceled)

17. (Previously Amended) The SOI structure according to claim 18, further comprising:
a gate defining a channel interposed between a source and a drain formed within an active region of the SOI structure; and
the active region defined in the semiconductor layer by isolation trenches and the LTCIM layer.

18. (Currently Amended) A semiconductor-on-insulator (SOI) structure comprising:
a semiconductor substrate;
a leaky, thermally conductive insulator material (LTCIM) layer disposed directly on the semiconductor substrate; and
a semiconductor layer disposed directly on the LTCIM layer,
wherein the LTCIM layer comprises at least one of doped amorphous silicon, undoped amorphous silicon and undoped porous silicon,
wherein when the LTCIM layer is doped amorphous silicon a dopant species is selected from one of boron, phosphorous and fluorine, and
wherein the LTCIM layer extends over an entire lateral dimension of the semiconductor substrate.

19. (Previously Added) The SOI structure according to claim 18 further including:
a gate defining a channel interposed between a source and a drain formed within an active region of the SOI structure.

20. (New) The SOI structure according to claim 1, wherein the semiconductor layer is germanium (Ge).

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21. (New) The SOI structure according to claim 20, wherein the semiconductor substrate material is silicon (Si), silicon carbide (SiC), silicon germanium (SiGe) or any other semiconductive material.

22. (New) The SOI structure according to claim 20, wherein the LTCIM layer has a thermally conductivity value between about 30 W/mK to about 170 W/mK.

23. (New) The SOI structure according to claim 20, wherein the LTCIM layer preferably has a resistivity value 10 Ohms-cm or greater.

24. (New) The SOI structure according to claim 18, wherein the semiconductor layer is germanium (Ge).

25. (New) The SOI structure according to claim 24, wherein the semiconductor substrate material is silicon (Si), silicon carbide (SiC), silicon germanium (SiGe) or any other semiconductive material.

26. (New) The SOI structure according to claim 24, wherein the LTCIM layer has a thermally conductivity value between about 30 W/mK to about 170 W/mK.

27. (New) The SOI structure according to claim 24, wherein the LTCIM layer preferably has a resistivity value 10 Ohms-cm or greater.